```
---Simplistic State machine for flash
---Target Board-Sparten3E
--Clock used for internal logic->50Mhz devided by 16
process(clk_out,reset_int)
begin
if (reset_int = '1') then
    Flash_we_n <= '1';
    Flash_oe_n <= '1';
    flash_cs_n<='1';
    count<=0;
    Flash_addr <= (others => 'Z');
    Flash_data <= (others => 'Z');
  state     <= rst_state;
    address_counter<=0;
elsif (clk_out='1' and clk_out'event) then
case state is
    when rst_state=>
            if(start='1')then
            state<=device_id_state;
            else
            state<=rst_state;
            end if;
when device_id_state=>
            Flash_addr <= (others => '0');
```

```
                Flash_data <=x"00FF";
                Flash_we_n <= '1';
                 Flash_oe_n <= '1';
                flash_cs_n<='1';
                state<=device_id_write0_FF;
when device_id_write0_FF=>
                Flash_we_n <= '1';
                 Flash_oe_n <= '1';
                  flash_cs_n<='0';
                state<=device_id_write1_FF;
when device_id_write1_FF=>
                Flash_we_n <= '0';
                 Flash_oe_n <= '1';
                  flash_cs_n<='0';
                state<=device_id_write2_FF;
 when device_id_write2_FF=>
                Flash_we_n <= '1';
                  Flash_oe_n <= '1';
                flash_cs_n<='0';
                state<=device_id_write3_FF;
 when device_id_write3_FF=>
                state<=device_id_write4_FF;
                Flash_we_n <= '1';
                 Flash_oe_n <= '1';
```

```
            flash_cs_n<='1';
when device_id_write4_FF=>          ---1 clock delay
            Flash_we_n <= '1';
            Flash_oe_n<='1';
            flash_cs_n<='1';
            Flash_addr <= (others => 'Z');
            Flash_data <=(others => 'Z');
            state<=device_id_write_90;
            ----Write x"90" to Flash Memory
when device_id_write_90=>
            Flash_addr <= (others => '0');
            Flash_data <=x"0090";
            state<=device_id_write0_90;
when device_id_write0_90=>
           Flash_we_n <= '1';
            Flash_oe_n <= '1';
           flash_cs_n<='0';
            state<=device_id_write1_90;
when device_id_write1_90=>
            Flash_we_n <= '0';
            Flash_oe_n <= '1';
            flash_cs_n<='0';
            state<=device_id_write2_90;
when device_id_write2_90=>
```

```
            Flash_we_n <= '1';
            Flash_oe_n <= '1';
           flash_cs_n<='0';
            state<=device_id_write3_90;
when device_id_write3_90=>
            state<=device_id_write4_90;
            Flash_we_n <= '1';
           Flash_oe_n <= '1';
           flash_cs_n<='1';
 when device_id_write4_90=>        ---delay  state
            Flash_we_n <= '1';
            Flash_oe_n<='1';
            flash_cs_n<='1';
            Flash_addr <= (others => 'Z');
            Flash_data <=(others => 'Z');
            state<=device_id_read;
 when device_id_read=>
            Flash_addr<=(others=>'0');
            Flash_data <=(others=>'Z');
            Flash_we_n <= '1';
            Flash_oe_n<='1';
            flash_cs_n<='1';
            state<=device_id_read0;
when device_id_read0=>
```

```
                Flash_we_n <= '1';
                Flash_oe_n<='1';
                flash_cs_n<='0';
                state<=device_id_read1;
 when device_id_read1=>          ---Read pulse for 2 clocks
                Flash_we_n <= '1';
                Flash_oe_n<='0';
                flash_cs_n<='0';
                state<=device_id_read2;
when device_id_read2=>
                Flash_we_n <= '1';
                Flash_oe_n<='0';
                flash_cs_n<='0';
                state<=device_id_read3;
when device_id_read3=>
                Flash_we_n <= '1';
                Flash_oe_n<='1';
                flash_cs_n<='0';
                state<=device_id_read4;
when device_id_read4=>
                Flash_we_n <= '1';
                Flash_oe_n<='1';
                flash_cs_n<='1';
                state<=wait_state;
```

```
when wait_state=>
            state<=wait_state;
 when others=>null;
end case;
end if;
end process;
```