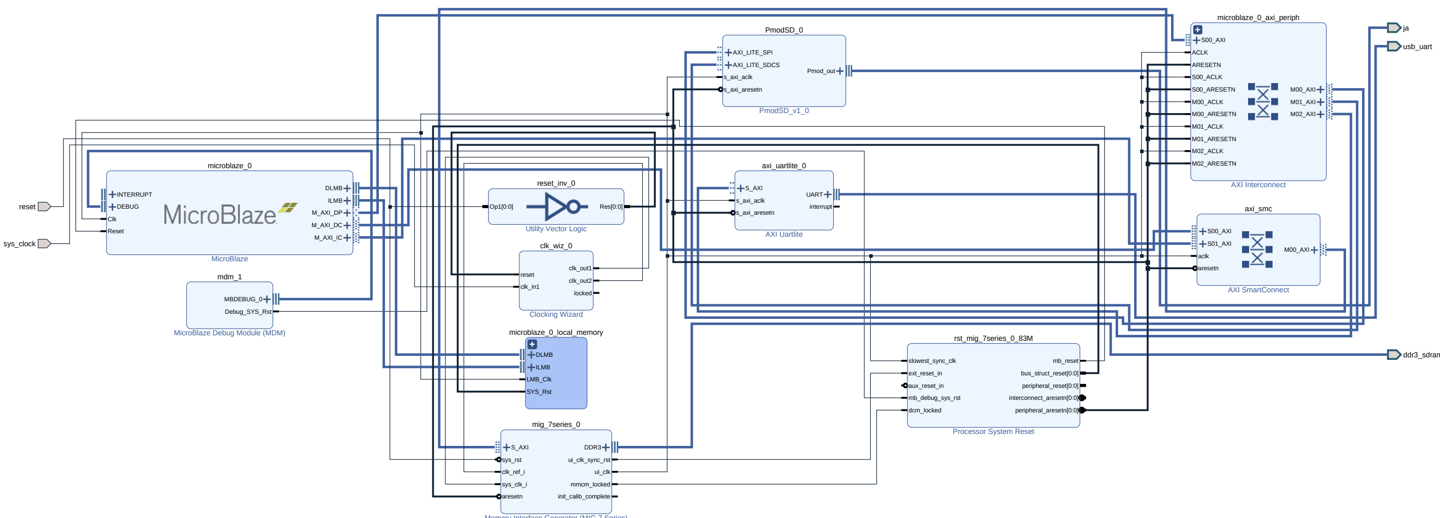

reset
sys_clock
microblaze_0
INTERRUPT
DEBUG
Clk
Reset
MicroBlaze
DLMB
ILMB
M_AXI_DP
M_AXI_DC
M_AXI_IC
MicroBlaze
mdm_1
MBDEBUG_0
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
reset_inv_0
Op1[0:0]
Res[0:0]
Utility Vector Logic
clk_wiz_0
reset
clk_in1
clk_out1
clk_out2
locked
Clocking Wizard
microblaze_0_local_memory
DLMB
ILMB
LMB_Clk
SYS_Rst
mig_7series_0
S_AXI
sys_rst
clk_ref_i
sys_clk_i
aresetn
DDR3
ui_clk_sync_rst
ui_clk
mmcm_locked
init_calib_complete
Memory Interface Generator (MIG 7 Series)
PmodSD_0
AXI_LITE_SPI
AXI_LITE_SDCS
s_axi_aclk
s_axi_aresetn
Pmod_out
PmodSD_v1_0
axi_uartlite_0
S_AXI
s_axi_aclk
s_axi_aresetn
UART
interrupt
AXI Uartlite
rst_mig_7series_0_83M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
microblaze_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M00_AXI
M01_AXI
M02_AXI
AXI Interconnect
axi_smc
S00_AXI
S01_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
ja
usb_uart
ddr3_sdram