**Results in Waveform Window of Debug ILA**

Output of Debug screen without EDID at Tx part of hdmi



Figure 1 : The count value for hsync signal is observed as 2156 which consist of 1920 of data

Remarks:

All the experiments were done at 1080p@60Hz



Figure 2 : Hsync, Vsync, Data of Inbuilt pattern to RGB2DVI IP

Output of Debug screen without EDID at RX part of HDMI



Figure 3 Observation :When Hsync signals is high and video enable signals also high



Figure 4: The Waveform window of ILA for RX part is same when DVI2RGB IP is enabled with EDID



Figure 5:The Waveform window of ILA for RX part is same when DVI2RGB IP is enabled with and without EDID

To monitor the pixel clock at TX and RX with EDID



Figure 6


Figure 7

Tx pixel clock is observed as 148.571430 MHz

Rx pixel clock is observed as 148.500352 MHz